Remarks

The Applicant agrees that the Japanese copies of priority documents are erroneous and belong to another application. Nonetheless, the Applicant respectfully submits that a proper claim of priority has been made with respect to FR00/03322, filed March 15, 2000. The Applicant submits herewith a certified copy of the French priority document.

The Applicant notes with appreciation the Examiner's helpful suggestion with respect to a new title. That suggested title has been adopted.

The Applicant acknowledges the rejection of Claims 15-21 and 23-28 under 35 U.S.C. §112. The Applicant respectfully submits that the rejection is now moot as it applies to Claims 27 and 28 in view of their cancellation. The remaining claims have been reviewed and where necessary, amended to provide a clear antecedent basis, and to remove phrases such as: "including", "and/or", "adapted for", and "adapting" from the claim language. Accordingly, the Applicant respectfully submits that Claims 15-21 and 23-26 are now in compliance with §112. Withdrawal of the rejection is respectfully requested.

The Applicant acknowledges the rejection of Claims 15-21 and 22-28 under 35 U.S.C. §102 as being anticipated by US Patent No. 6,446,192 to Narasimhan et al., hereinafter "the '192 patent". The Applicant respectfully submits that the rejection is now moot as it applies to Claims 27 and 28 in view of their cancellation. The Applicant nonetheless respectfully submits that the remaining claims are fully patentable over the '192 patent for the reasons set forth below.

Independent Claim 15, as amended, recites:

> An electronic component for connecting to and exchanging data with a telecommunications network, the electronic component comprising a DSP (Digital Signal processor) which DSP further comprises:
>
> at least one memory in which is loaded a program for implementing an Internet

protocol array and for running at least one of a message handling routine, a FTP download routine and a routine providing Web server functionalities;

a signal processing program for exchanging data on a telecommunications network; and

a supervisory layer software for: converting data exchanged between the DSP and a communications device into data messages exchanged with a remote system; automatically generating outgoing calls to an internet service provider (ISP); and confirming whether a datum has been sent to the remote system;

wherein the protocol array, the signal processing program, and the supervisory layer software are jointly integrated in the DSP. (emphasis added).

As emphasized above, Claim 15 recites the joint integration of a protocol array, a signal processing program, and a supervisory layer software in a single DSP. The Applicant respectfully submits that the '192 patent fails to disclose, either explicitly or implicitly, that the program implementing internet functions (i.e., the protocol array) is loaded in the memory of a DSP. In particular, the SMTP, FTP and HTTP routines of Fig. 2 of the '192 patent are stored in the Network interface chip 36. This is not a DSP as specifically recited in Claim 15. As noted in the '192 patent at column 6, lines 14-21, the device control circuitry 38, which may include a DSP according to line 21, has "little or no networking capability." Furthermore, the '192 patent in Fig. 12 discloses a UART (Universal Asynchronous Receiver/Transmitter) for connecting chip 36 to a modem. Thus, chip 36 cannot be considered to be a modem chip inasmuch as it does not comprise modem functionalities.

The '192 patent also fails to disclose supervisory layer software being integrated into a single DSP. At col. 3, line 9-et seq., the '192 patent discloses a single integrated circuit chip for interfacing device control circuitry (which may contain a DSP) to a client machine via a computer network. The single integrated chip of the '192 patent includes interfaces for communicating with device control circuitry and with a computer network. Unlike the single chip of '192 patent, however, Claim 15

recites these and additional supervisory functions being run from a supervisory layer software in the DSP. As known to those skilled in the art, and as disclosed in the '192 patent, supervisory layer software functions are conventionally found on the application layer, and not on a DSP. Furthermore, the single chip of the '192 patent fails to disclose the supervisory functions of: converting data communicated between the DSP and a device into a message for exchanging with a remote system; generating outgoing calls from the DSP to an internet service provider (ISP); and confirming whether a datum has been sent to a remote system.

The DSP as recited in Claim 15 is sharply contrasted to single chip of the '192 patent since it comprises a memory in which is loaded an Internet protocol array, a signal processing program, and supervisory layer software. The '192 patent does not explicitly or implicitly disclose a DSP comprising such programs. The DSP of the '192 patent discloses in column 6, line 21 is in the device control circuitry 38, and does not comprise a memory in which is loaded an Internet protocol array or a supervisory layer software. The Applicant therefore respectfully submits that Claims 15-21 and 23-26 are patentable over the '192 patent. Withdrawal of the §102 rejection is respectfully requested.

The Applicant acknowledges the rejection of Claims 15-22 and 23-28 under 35 U.S.C. §103 over the '192 patent. The Applicant respectfully submits that the rejection as it applies to Claims 27 and 28 is moot in view of the cancellation of Claims 27 and 28. The Applicant also respectfully submits that Claims 15-21 and 23-28 are patentable over the '192 patent for the reasons set forth below.

As noted above, Claim 15 recites, among other things, the program for implementing a protocol array, the signal processing program, and the supervisory layer software are jointly

integrated into a single DSP. The Applicant respectfully submits that there is utterly no teaching or suggestion for one skilled in the art to modify the '192 patent and to integrate the whole of the circuitry of Fig. 1b, the network interface functionalities, and the supervisory functionalities into a single DSP, as recited in Claim 15.

This rejection relies on the notion that the integration of the circuitries of Fig. 1b of the '192 patent into a single monolithic chip was to reduce chip count, pin I/O and size. However, the Applicant notes that in view of the '192 patent there is no teaching or suggestion to reduce chip count, pin I/O and/or size. In fact, the '192 patent teaches a single web interfacing chip and, accordingly, nothing in the '192 patent teaches or suggests that data processing functionalities and/or supervisory functionalities can be integrated into such a chip.

Instead, the '192 patent teaches a first chip comprising Internet functionalities and a second chip which may comprise a DSP. In column 6 at lines 14 and 15 , the '192 patent teaches that "the device control circuitry 38 implements the main functionality of the device 34, that typically has little or no network capability." The network interface chip 36 "...implements all network services..." (see col. 6, lines 30-46 of the '192 patent). This dual-chip teaching is the opposite of the subject matter recited in Claims 15-21 and 23-26, which recites the integration of Internet functionalities, signal processing, and supervisory functionalities into a single DSP. Accordingly, the Applicant respectfully submits that Claims 15-21 and 23-26 are non-obvious in view of the '192 patent. Withdrawal of the §103 rejection is respectfully requested.

In light of the foregoing, the Applicant respectfully submits that the entire application, including Claims 15-21 and 23-26, is now in condition for allowance, which is respectfully requested.

Respectfully submitted,

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